Patent Claims

1. An integrated circuit arrangement (140), having an electrically insulating insulating region, and having at least one sequence of regions which forms a capacitor (144) and which contains, in the order specified:
an electrode region (34) near the insulating region,
a dielectric region (46), and
an electrode region (56) remote from the insulating region,
the insulating region being part of an insulating layer (14) arranged in a plane,
the capacitor (144) and at least one active component (142) of the integrated circuit arrangement (140) being arranged on the same side of the insulating layer (14), and the electrode region (34) near the insulating region and the active region (84) of the component (142) being arranged in a plane which lies parallel to the plane in which the insulating layer (14) is arranged.

2. The circuit arrangement (140) as claimed in claim 1, characterized by at least one field-effect transistor (142), whose channel region (84) is the active region, the channel region (84) preferably being doped or undoped,
and/or whose control electrode (54) contains the same material and/or material of the same dopant concentration as the electrode region (56) remote from the insulating region,
and/or whose control electrode insulating region (42) contains the same material and/or a material having the same thickness as the dielectric region (46),
and/or whose control electrode insulation region (42) contains a different material and/or a material having a different thickness than the dielectric region (46).

3. The circuit arrangement (140) as claimed in claim 2, wherein the field-effect transistor (122) is a planar field-effect transistor,
and/or wherein the transistor contains auxiliary terminal regions (58, 59), which have a doping with the same conduction type as the terminal regions (80, 82) but with a dopant concentration that is smaller by at least one order of magnitude,
and/or wherein the transistor contains auxiliary doping regions, which are arranged near the terminal regions (80, 82) and/or near the auxiliary terminal regions (58, 59) and which have a doping with a different conduction type than the terminal regions (80, 82) and/or than the auxiliary terminal regions (58, 59),
and/or wherein the control electrode (54) adjoins a region containing a metal-semiconductor compound, in particular a silicide region (92).

4. The circuit arrangement (140) as claimed in claim 2 or 3, wherein one terminal region (80, 82) of the transistor (142) or both terminal regions (80, 82) of the transistor (142) adjoin the insulating layer (14),
and/or wherein at least one terminal region (80, 82) adjoins a region containing a metal-semiconductor compound, preferably a silicide region (90, 96),
and/or wherein a boundary area of at least one terminal region (80, 82) which is remote from the insulating region is further away from the insulating layer (14) than the active region (84), or
wherein a boundary area of at least one terminal region (80, 82) which is remote from the insulating region is arranged nearer to the insulating layer (14) than a boundary area of the active region (84) which is remote from the insulating region.

5. The circuit arrangement (140) as claimed in one of claims 2 to 4, wherein spacers (60, 62) are arranged on

both sides of the control electrode (54), which spacers contain a different material than the control electrode (54), preferably silicon dioxide or silicon nitride, or which spacers comprise a different material than the control electrode (54), preferably silicon dioxide or silicon nitride,
and/or wherein a spacer (64, 66) is arranged at at least one side of the electrode region (56) remote from the insulating region, which spacer contains a different material than the electrode region (56) remote from the insulating region, preferably silicon dioxide or silicon nitride, or which spacer comprises a different material than the electrode region (56) remote from the insulating region, preferably silicon dioxide or silicon nitride,
and/or wherein a spacer (62a) arranged at the control electrode (54) and a spacer (64a) arranged at the electrode region (56) remote from the insulating region touch one another.

6. The circuit arrangement (140) as claimed in one of claims 2 to 5, wherein a terminal region (82) of the field-effect transistor (142) and the electrode region (34) of the capacitor (144) which is near the insulating region adjoin one another and have an electrically conductive connection at the boundary,
and/or wherein the terminal region (59a) of the transistor (152) which adjoins the electrode region (34) near the insulating region does not adjoin a region containing a metal-semiconductor compound, in particular does not adjoin a silicide region,
and/or wherein the other terminal region (80a) adjoins a region (70a) containing a metal-semiconductor compound.

7. The circuit arrangement (140) as claimed in claim 6, wherein that side of the electrode region (34) near the insulating region which adjoins the terminal region

(82) is longer than a side of the electrode region (34) near the insulating region which lies transversely with respect to said side, preferably being at least twice as long or at least five times as long,
the transistor (142) preferably having a transistor width (W1) which is a multiple of the minimum feature size (F), preferably more than three-fold or more than five-fold,
or wherein a side of the electrode region (34) near the insulating region which lies transversely with respect to that side of the electrode region (34) near the insulating region which adjoins the terminal region (82) is longer than the side adjoining the terminal region (82), preferably at least twice as long or at least five times as long,
the transistor (152) preferably having a transistor width (W2) which is less than three times the minimum feature size (F), preferably less than twice the minimum feature size (F).

8. The circuit arrangement (140) as claimed in one of the preceding claims, wherein the electrode region (34) near the insulating region is a monocrystalline region, preferably a doped semiconductor region,
and/or wherein the electrode region (34) near the insulating region and/or the active region (84) has a thickness of less than 100 nanometers or less than 50 nanometers,
and/or wherein the active region (84) is a monocrystalline region, preferably a semiconductor region which is doped or undoped,
and/or wherein the insulating layer (14) adjoins, at one side, a carrier substrate (12), preferably a carrier substrate which contains a semiconductor material or comprises a semiconductor material in particular silicon or monocrystalline silicon,

and/or wherein the insulating layer (14) adjoins the electrode region (34) near the insulating region at the other side,
and/or wherein the boundary areas preferably lie completely in two mutually parallel planes,
and/or wherein the insulating layer (14) contains an electrically insulating material, preferably an oxide, in particular silicon dioxide, or comprises an electrically insulating material, preferably an oxide, in particular silicon dioxide,
and/or wherein the active component (142) is a transistor, preferably a field-effect transistor, in particular a planar field-effect transistor.

9. The circuit arrangement (140) as claimed in one of the preceding claims, wherein the dielectric region (46) contains silicon dioxide or comprises silicon dioxide,
and/or wherein the dielectric region (46) comprises a material having a dielectric constant of greater than 4 or greater than 10 or greater than 50,
and/or wherein the electrode region (56) remote from the insulating region contains silicon, preferably polycrystalline silicon, or comprises silicon, preferably polycrystalline silicon,
and/or wherein the electrode region (56) remote from the insulating region contains a metal or comprises a metal,
and/or wherein the electrode region (56) remote from the insulating region contains a low-impedance material, preferably titanium nitride, tantalum nitride, rubidium or highly doped silicon-germanium,
and/or wherein the electrode region (56) remote from the insulating region adjoins a region containing metal-semiconductor compounds, in particular a silicide region (96).

10. The circuit arrangement (140) as claimed in one of the preceding claims, wherein the circuit arrangement contains at least one processor, preferably a microprocessor,
and/or wherein the capacitor (154) and the active component (152) form a memory cell (150), in particular in a dynamic RAM memory unit,
and/or wherein a memory cell contains either a capacitor (152) and only one transistor (152) or a capacitor (Cs) and more than one transistor (M1 to M3), preferably three transistors (M1 to M3).

11. A method for fabricating an integrated circuit arrangement (140) with a capacitor (144), in particular a circuit arrangement (140) as claimed in one of the preceding claims,
in which the following method steps are performed without any restriction by the order specified:
provision of a substrate (10) containing an insulating layer (14) made of electrically insulating material and a semiconductor layer (16),
patterning of the semiconductor layer (16) in order to form at least one electrode region (34) for a capacitor and in order to form at least one active region (84) for a transistor (142),
after the patterning of the semiconductor layer (16) production of at least one dielectric layer (42, 46),
after the production of the dielectric layer (42, 46) production of an electrode layer (41),
formation of an electrode (56) of the capacitor (144) which is remote from the insulating region in the electrode layer (41).

12. The method as claimed in claim 11, characterized by the following steps:
application of at least one auxiliary layer (18, 20) to the semiconductor layer (16) prior to patterning, preferably a silicon nitride layer (20) and/or an oxide

layer (18), the auxiliary layer (20) preferably serving as a hard mask during the patterning of the semiconductor layer (16),
and/or doping of a channel region (84) of the transistor (142), preferably before the production of the dielectric layer (42, 46),
carrying out of a thermal oxidation in order to form a rounding oxide (26, 28), preferably before the formation of the electrode layer (41),
and/or doping of the electrode (34) near the insulating region, preferably before the production of the dielectric layer (42, 44, 46),
and/or production of the dielectric layer (42, 46) at the same time as a dielectric layer at the active region (84) of the transistor (122),
and/or formation of a control electrode (54) of the transistor (142) at the same time as the formation of the electrode region (56) remote from the insulating region.

13. The method as claimed in claim 11 or 12, characterized by the following steps:
formation of auxiliary terminal regions (58, 59) with a lower dopant concentration than terminal regions (80, 82) of the transistor (142), preferably after the patterning of a control electrode (54) of the transistor (142),
and/or formation of auxiliary doping regions, preferably before the patterning of the control electrode (54),
application of a further auxiliary layer (60 to 66) after the patterning of a control electrode (54) of the transistor (142), preferably a silicon nitride layer or a silicon dioxide layer, in particular a TEOS layer,
and/or anisotropic etching of the further auxiliary layer (60 to 66).

14. The method as claimed in one of claims 11 to 13, characterized by the following steps:
carrying out of a selective epitaxy on uncovered regions made of semiconductor material (16) after the formation of the electrode region (56) remote from the insulating region and/or after the patterning of a control electrode (54) of the transistor (142),
and/or doping of terminal regions (70, 72) of the transistor (122) after the formation of the electrode region (56) remote from the insulating region and/or after the patterning of the control electrode (54) and preferably after the epitaxy.

15. The method as claimed in one of claims 11 to 14, characterized by the following step:
and/or selective formation of a metal-semiconductor compound, in particular selective silicide formation, on the electrode layer (54) and/or on uncovered semiconductor regions (16).

List of reference symbols

I, II	Sectional plane
10	SOI substrate
12	Carrier substrate
14	Insulating layer
16	Semiconductor layer
16a	Transistor part
16b	Capacitor part
18	Silicon dioxide layer
20	Silicon nitride layer
22	Photoresist layer
24	Layer stack
26, 28	Oxide rounding sections
30, 32	Photoresist layer
33	Implantation
34	Bottom electrode region
40	Silicon dioxide layer
41	Polysilicon layer
42	Gate oxide
46	Dielectric
50a, 50b	Photoresist layer region
54	Gate electrode
56	Covering electrode
57	Implantation
58, 59	LDD region
60 to 66	Spacers
70 to 76	Epitaxial region
78	Implantation
80, 82	Source/Drain region
84	Channel region
90 to 96	Silicide region
100	Passivation layer
102 to 136	Connecting section
140	Transistor-capacitor arrangement
142	Field-effect transistor
144	Capacitor
W1, W2	Transistor width

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L1, L2	Length
B1, B2	Width
A	Area
F	Minimum feature size
150	Memory cell
152	Field-effect transistor
154	Capacitor
200	Memory cell
M1 to M3	Transistor
Cs	Capacitor
BL1	Write bit line
BL2	Read bit line
RWL	Read word line
WWL	Write word line
X	Storage node
VDD	Operating potential
VSS	Ground potential